ARRAYS: THE ULA

The ULA provides a fast and low cost route to high performance custom LSI/VLSI.

The timescale into production is short and prices are competitive from small to very large volumes.

A family of digital ULA's covers system complexities of up to 10,000 gates and requirements from ECL speeds to CMOS power levels.

A family of Digilin ULA's are designed to provide high complexity digital and high performance linear functions on the same chip.

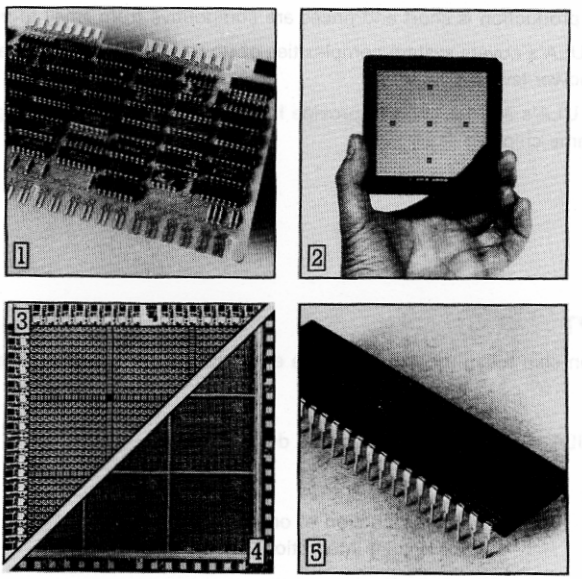
ULA CONCEPT

The ULA is a silicon chip fully processed with the exception of a single layer interconnection pattern.

Every chip in the ULA family employs a common design concept.

- The production of only a single mask for system integration.
- An "on-chip" component interconnection technique giving high chip utilisation and complexity.
- A regular matrix of cells. Each cell containing a number of uncommitted components whose prime function is to satisfy the logic hierarchy of an LSI system.
- Peripheral cells also containing a number of uncommitted components to facilitate interfacing with all other commonly used device technologies: bipolar, MOS and CMOS, and the implementation of high performance linear functions.

ARRAYS: THE ULA



1. Customers existing or proposed MSI system.
2. Single ULA interconnection mask derived from MSI system.
3. Uncommitted ULA chip held as stock item.
4. ULA chip completed using single layer interconnection mask.
5. Finished ULA LSI product.

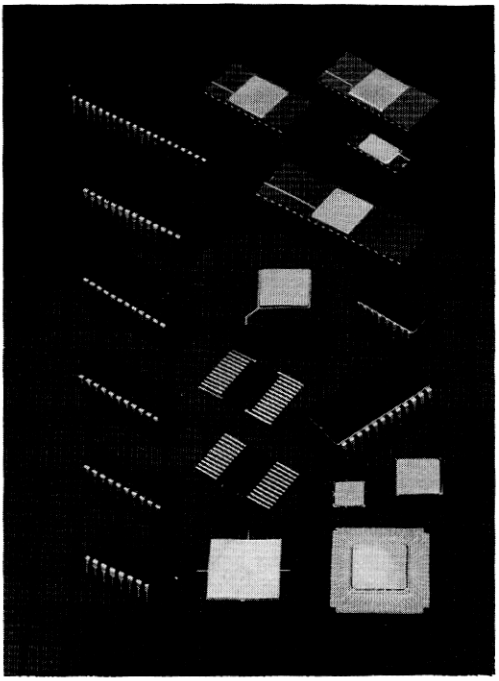
The Ferranti ULA provides an economic LSI solution to a customer's requirement in a fixed, fast and dependable timescale, whatever the market sector.

The ULA family is a range of bipolar LSI chips. Each chip contains an array of 'uncommitted' active and passive components fully processed except for the final, single layer, aluminium interconnection stage.

The interconnection pattern connecting the individual components to provide system integration, is generated from the user's specification either by Ferranti or by the customer himself.

The functional packing density is equivalent to full custom design, and the ULA is therefore competitive at all volume levels, including very large volume.

ARRAYS: THE ULA



Finished Product

The ULA is designed to operate over the military temperature range −55°C to +125°C, thus embracing the various industrial temperature ranges.

The package in which the ULA chip is supplied can be plastic or ceramic dual in-lines, flat-packs or chip carriers ranging from 14 to 68 pins.

ULA PERFORMANCE

All ULAs have the facility for combining both digital and linear functions on the same chip, providing the opportunity for total system integration. The range of ULAs enables an LSI/VLSI solution to be realised with system complexities of up to 10,000 gates.

DIGITAL PERFORMANCE

All commonly used logic functions can be implemented with system clock gates up to, and under correct conditions in excess of 60MHz.

LINEAR PERFORMANCE

A very extensive range of high performance linear functions can be implemented such as precision references, voltage regulators, comparators, op-amps, analogue switches, oscillators and A/D converters, etc.

INTERFACE CAPABILITY

The uncommitted components available in both the matrix and peripheral cells provide I/P and O/P interfacing capability for TTL, MOS and CMOS technologies, triacs, relays, LEDs and LCDs, transistors, phototransistors, switch and toch switch inputs, etc.

ARRAYS: THE ULA

PRODUCT DATA SUMMARY — ULA GATE ARRAYS

Array Type	Gate Count	Clock Rate (MHz)	Gate Delay (ns)	Gate Power (μW)	Package Pin Count
ULA2N	450	6	25.0	70	14 to 40
ULA2C	450	20	8.0	250	14 to 40
ULA5RC	500	10	15.0	30	24 to 40
ULA5RB	500	20	7.5	100	24 to 40
ULA5RA	500	60	2.5	300	24 to 40
ULA5N	900	6	25.0	70	24 to 68
ULA5C	900	20	8.0	250	24 to 68
ULA9RC	900	10	15.0	30	24 to 68
ULA9RB	900	20	7.5	100	24 to 68
ULA9RA	900	60	2.5	300	24 to 68
ULA12RC	1200	10	15.0	30	24 to 68
ULA12RB	1200	20	7.5	100	24 to 68
ULA12RA	1200	60	2.5	300	24 to 68
ULA16RC	1600	10	15.0	30	24 to 68
ULA16RB	1600	20	7.5	100	24 to 68
ULA16RA	1600	60	2.5	300	24 to 68
ULA18RC	1800	10	15.0	30	24 to 68
ULA18RB	1800	20	7.5	100	24 to 68
ULA18RA	1800	60	2.5	300	24 to 68
ULA9C	2000	20	8.0	120	24 to 68
ULA20RC	2000	10	15.0	30	24 to 68
ULA20RB	2000	20	7.5	100	24 to 68
ULA20RA	2000	60	2.5	300	24 to 68
ULA24RC	2400	10	15.0	30	24 to 68
ULA24RB	2400	20	7.5	100	24 to 68
ULA24RA	2400	60	2.5	300	24 to 68

ADVANCED PRODUCT INFORMATION (available for design during 1982)

ULA40RA	4000	60	2.5	300	40 to 68
ULA100RA	10000	60	2.5	300	40 to 68

PRODUCT DATA SUMMARY — ULA DIGILIN ARRAYS

Array Type	Gate Count	Gate Power (μW)	No. of Active Components	No. of Passive Components	Package Pin Count
ULA1G	100	1.9	356	531	14 to 28
ULA1L	150	180.0	384	696	14 to 28
ULA2G	160	1.9	647	704	14 to 30
ULA1U	280	3.4	676	741	14 to 40
ULA2L	340	200.0	715	1205	14 to 40
ULA2M	500	0.4	1184	968	14 to 40
ULA2U	510	3.4	1152	1096	14 to 40
ULA3U	580	3.4	1348	1443	14 to 40
ULA5L	730	200.0	1644	2660	24 to 40

The number of active and passive components given in the table above are the total number of components contained in both the matrix and peripheral cells. The data sheet for each array should be consulted for the precise component content. However, each array contains a variety of transistors from high gain, low current devices to 100mA drive transistors. The resistors range in value from 100Ω to 1MΩ. Many of the arrays contain on-chip bandgap references, series and shunt regulators, shaping capacitors, etc.

SUPPLY VOLTAGE

The Digilin ULA's are designed to operate from supply voltages of 1.0V to 5.5V whilst the ULA gate arrays will operate from 3.3V to 5.5V. By suitable interconnection of the on-chip components, regulation is readily achieved allowing the ULA's to operate from any supply rail by using minimal external components.

ARRAYS: THE ULA

ULA DESIGN ROUTE

Only one interconnection mask is needed to convert the uncommitted ULA chip to the required Custom LSI circuit. Development costs are therefore low and development and production lead times are very short. The ULA design can be carried out by Ferranti or the customer supported by one of the most advanced ULA CAD facilities in operation.

Over 40 man years of ULA specialised automation software is available and in use. The software programmes include layout and design rule checking, logic checking and simulation, automatic layout aids, high level test language and test programme and test schedule verification.

THE ULA DESIGNER

The ULA Designer is an interactive design system consisting of a powerful minicomputer, edit terminal, control console, digitiser and plotter. Installed in the customer's premises it provides the customer's engineer with all the CAD facilities necessary to specify, design and verify ULA LSI and VLSI circuits.

N.B. "ULA Designer" is a trademark of Ferranti plc.

Design by Ferranti: The customer provides system specification and description including logic diagram and Ferranti carry out the complete ULA design cycle.

Design by Customer: There are three design options fully supported by comprehensive documents, design manuals and design courses, available to the customer who needs to carry out his own ULA design.

OPTION 1

The customer provides an integration package of logic diagram, layout routing and test and device specification.

OPTION 2

The customer who has installed the ULA DESIGNER carries out the complete design cycle on his own premises. When the design is complete and verified, the layout, logic and test schedules are transmitted via a modem link to the ULA CAD Complex for prototype manufacture.

OPTION 3

ULA software programmes can be purchased for customers with Applicon and Calma Graphics Systems. Interface to the Ferranti ULA CAD Complex is by magnetic tape.

ARRAYS: THE MONOCHIP

The Monochip range of arrays is designed to facilitate the design and manufacture of linear custom LSI. The range consists of ten standard chip designs each containing a large number of integrated components (npn and pnp transistors, and resistors) on fixed locations. All that is required to complete a custom circuit is the aluminium interconnection layer.

The basic processing is identical for all Monochip circuits with only the aluminium interconnection custom designed. Short development and production timescales result from this single mask customisation.

COMPONENT LIST FOR LINEAR MONOCHIPS

Type	MOA	MOB	MOC	MOD	MOE	MOF	MOG	MOH	MOJ	MOL	MOM
NPN Transistor, small	57	69	22	50	48	92	58	70	36	76	137
NPN Transistor, 100mA								2	2	2	4
NPN Transistor, 200mA	2					4	2			2	4
NPN Transistor, low noise											4
PNP Transistor, single	18	12	8								
PNP Transistor, dual				16	15	36	18	22	12	22	44
PNP Transistor, quad										4	8
PNP Transistor, vertical											4
Schottky Diodes	15	16	6								
15Ω N+ Resistors								4		8	15
Base Resistors											
200Ω	16	27	8	15	8	18	19	29	8	23	60
450Ω	43	44	18	30	32	88	68	82	34	103	188
900Ω	43	45	20	28	28	68	65	75	30	77	140
1.8kΩ	29	39	13	29	25	61	44	54	24	53	104
3.6kΩ	28	36	12	24	26	61	27	36	20	36	84
Total Base Resistance (kΩ)	214	265	94	180	180	433	269	337	159	345	712
Pinch Resistors											
30kΩ B/E	4	6	2		5	9					
100kΩ B/E	4	6									
2×60kΩ B/E							4	4	2	5	8
60kΩBulk				2							
Pads	16	24	14	16	18	24	18	18	18	24	28
Size (mils)	71×81	81×81	51×56	80×80	70×70	91×110	75×78	77×88	61×65	81×100	101×151

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . MOA to C, E to M 20V MOD 36V

Storage Temperature . . . . . −66°C to +150°C

Operating Temperature . . . . . Any range between −55°C and +125°C (depending on design requirements)

MONOCHIP COMPONENTS

NPN TRANSISTORS

All linear Monochips contain large numbers of NPN transistors. With gains from 80 to 300, useful collector current from 10nA to 20mA and an f_T of 500MHz, these NPN's are the building blocks of linear design.

HIGH CURRENT NPN TRANSISTORS

Larger interdigitated NPN transistors are available on some arrays.

PNP TRANSISTORS

Lateral PNP transistors are on all linear Monochips. Some arrays have PNP transistors with split collectors. This effectively doubles their usefulness thereby creating a single structure to work as an active load or current mirror. Gains are between 5 and 80 and useful collector current from 10nA to 2mA. An f_T of 3MHz limits their use to low frequency operation.

DIODES

Diodes are formed by connecting the base and collector contacts together. For reverse voltages below 6V an NPN type is used. At higher reverse voltage a PNP transistor must be used.

ZENER DIODES

The reverse voltage breakdown of the base emitter junction can be used as a Zener diode with a breakdown voltage between 6 and 7.2 volts.

RESISTORS

Diffused resistors are in five basic values. The lowest value of 200Ω serves mainly as a crossunder or balancing resistor. The higher values are arranged in a 1.2.4.8 ratio so that a large range of values can be generated by series and parallel connection. The absolute tolerance of diffused resistors is ±25% but the ratio matching is very good.

LARGE VALUE RESISTORS

Pinch resistors can be found on all arrays. They have a breakdown limitation of 6V.

THE MONOCHIP DESIGN KIT

The Monochip design kit is available to designers who wish to undertake a linear custom LSI design. The kit contains a handbook, breadboarding parts and some layout aids. The handbook describes the techniques of Monochip design with worked examples, circuit blocks and component parametric data. Circuit design can be checked by breadboarding using the kit parts. Colour printed layout sheets are provided, on request, to enable the interconnection to be designed.

The Monochip is presented as a kit to give the circuit designer a cost and time effective route to production custom linear LSI.